

WHAT IS CLAIMED IS:

1. A frequency divider enabling the division by N of a frequency F_e and comprising at least one prescaler followed by a division chain, wherein:

- the prescaler has at least one input for the frequency signal F_e to be divided, one input for a command NA of the basic division rank of the prescaler and one input for a command ΔNA coming from the division chain and enabling NA to be made to vary by one unit,
- the division chain comprises at least one division stage (K) comprising at least one divider by 2, giving a divided frequency $F(K)$, a switch controlled by the divider by 2, the switch having one input for a piece of programming data $R(K)$, one input for the carry signal $RX(K+1)$ of the next stage and one output for the carry signal $RX(K)$ for the previous stage.

2. A frequency divider according to claim 1 wherein the command NA varies from N_0 to $2 \cdot N_0 - 1$.

3. A frequency divider according to claim 2 wherein the command NA varies from 2^P to $2^{(P+1)} - 1$.

4. A frequency divider according to claim 1 comprising a first chain of switches controlled by the outputs $F(K)$ of the dividers and giving a signal $MC(P+1)$, a second chain of switches controlled by the outputs $F(K)$ of the dividers and giving a signal $TC(P+1)$ and a unit for the generation of a synchronous output prepared from the signals $TC(P+1)$, $MC(P+1)$ and the input signal $F(P)$ or output signal F_e of the prescaler.

5. A frequency divider according to claim 4 wherein the generation module is a JK type flip-flop circuit that receives the signals $MC(P+1)$ and $TC(P+1)$ and F_e or $F(P)$.

6. A frequency divider according to claim 4 comprising at least one second chain of switches controlled by the outputs $F(K)$ of the dividers and giving a signal $TC(P+1)$, at least two switches receiving the signal $TC(P+1)$

and giving two signals to a flip-flop circuit receiving the input signal or the output signal of the prescaler.

7. A frequency divider according to claim 4 comprising a first row of registers controlled by the intermediate outputs of the chain TC and a second row of registers controlled by the signal MC(P+1).

8. A frequency divider according to claim 4, comprising:

- a function for the taking into account in mid-frame of the division rank for the next frame, this function receiving the write signal MC(P+1),
- a function preparing the signal for taking account of the new division rank NA of the prescaler,
- a decoding function 44 enabling the extraction of the pieces of information NEXT_R(K), NEXT_ACT(K) and NEXT_NA from the control word N.

9. A frequency divider according to claim 8, comprising a function for taking account of the polarity of the synchronous output signal for the next frame.

10. A use of the divider according to claim 1 in the field of phase-locked loop frequency synthesis.

11. A use of the divider according to claim 1 for a pulse generator.